MediaGX™ Architectural System Overview

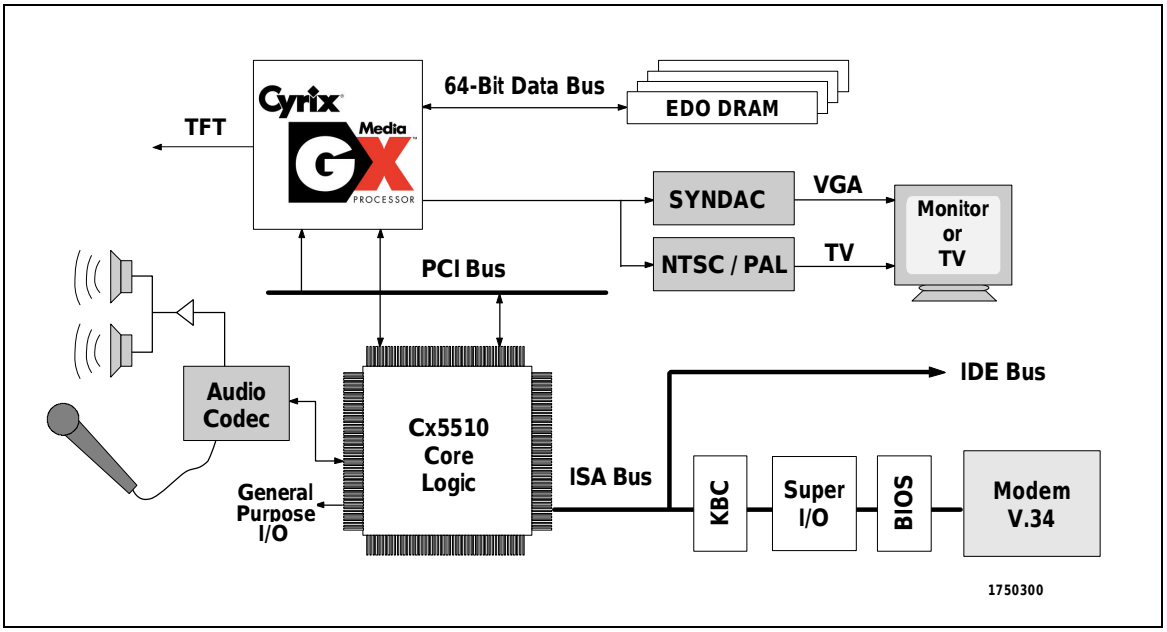
The Cyrix MediaGX™System establishes a new class of low-cost, high-performance desktop and notebook PC computers. This system eliminates the traditional audio and video cards, and all AT motherboard components of a PC.

The MediaGX System consists of two chips—the MediaGX processor and the MediaGX Cx5510 companion chip.

The audio and graphics functions of the two chips operate under the control of the Virtual System Architecture™ (VSA™) design. This design eliminates system conflicts and end-user configuration problems.

The MediaGX processor is a 64-bit data bus, x86-compatible processor with a proven core. The CPU directly interfaces to a PCI bus and DRAM memory. High quality SVGA is provided by an advanced graphics accelerator on the MediaGX processor. The graphics frame buffer is stored in main memory without the performance degradation associated with traditional Unified Memory Architecture (UMA) system designs due to Cyrix's new Display Compression Technology (DCT).

The companion chip, the MediaGX Cx5510, represents a new generation of integrated, single-chip controllers for Cyrix's line of MediaGX-compatible 64-bit processors. The Cx5510 bridges the MediaGX processor over the PCI bus to the ISA bus, performs traditional chip-set functions, and supports a full feature Sound Blaster® compatible sound interface.



MediaGX™ Processor Feature Summary

♦ 64-Bit x86 Processor
- PR133 Performance at 133 MHz
- 16 KByte Unified L1 Cache
- Unique Scratchpad RAM for SMM and Graphics
- Integrated Floating Point Unit
- Enhanced System Management Mode (SMM)

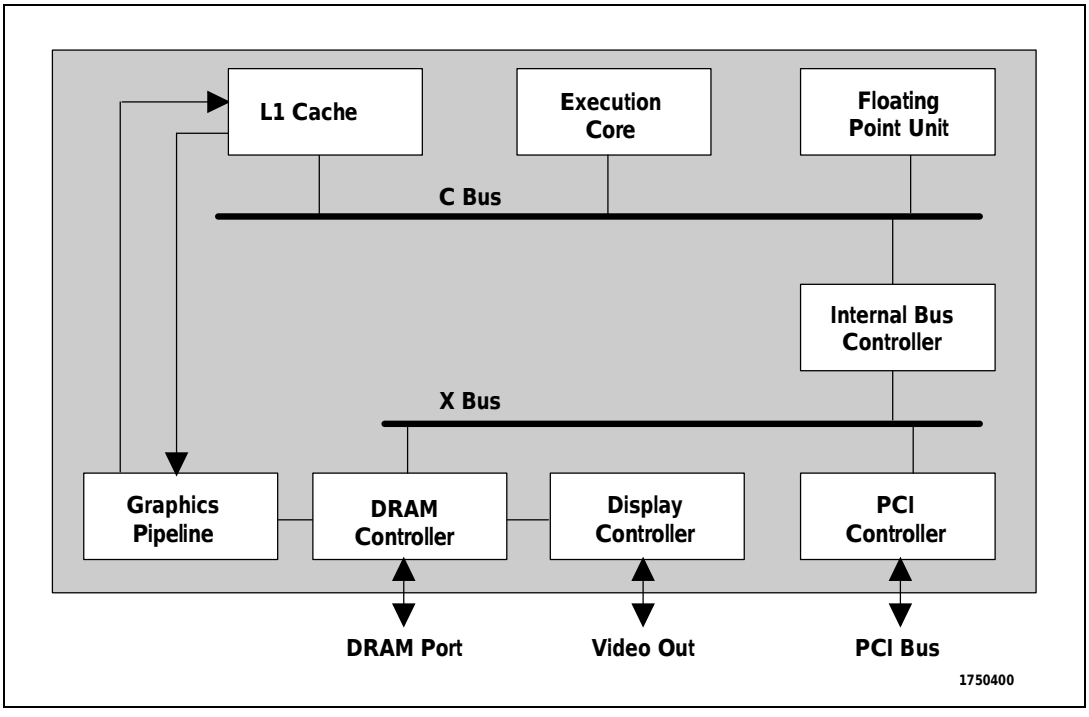
♦ Power Management
- Supports Cx5510 NoteBook Power Management
- Private Link to Cx5510 for Monitoring System Activity

♦ PCI Controller
- Fixed, Rotating, Hybrid or Ping Pong Arbitration
- Supports Four Masters (Three on PCI Bus)
- Synchronous CPU/PCI Bus Frequency
- Supports Concurrent CPU and PCI Operations

♦ Additional Features
- 352-Pin Ball Grid Array (BGA) Package
- 0.5 micron, TLM CMOS Process
- 3.3 to 3.6 Volt Operation

♦ VSA Virtual VGA
- Supports all VGA Modes
- Faster than Many Hardware-Based solutions
- Supports all VESA Modes
- Accelerates BitBLTs, Line Draw, Text
- Supports all 256 Raster Operations
- Runs at Core Clock Frequency
- Provides glueless TFT and RAMDAC Interface
- Supports up to 1280 x 1024 x8 and 1024 x 768 x 16 BPP

♦ Memory Subsystem
- 64-bit EDO DRAM Controller
- Tight Coupling to CPU Core
- Runs at Core Clock Frequency
- UMA Implemented with Video Compression
- CAS Before RAS and Self Refresh Support
- Provides Support for up to 128 MBytes in 4 Banks



MediaGX™ Processor Overview

MediaGX™ Processor

The MediaGX processor not only executes x86 instructions using a proven Cyrix CPU core, it also acts as a virtual video card. This chip provides a high-quality video port that connects directly to a flat panel or to an external RAMDAC chip for CRT display. The processor also provides a 64-bit wide DRAM interface and video compression which allows video and main memory sharing without memory performance degradation.

The MediaGX processor core operates from a 3.3 or 3.6 volt power supply, resulting in low power consumption at all clock frequencies. Where additional power savings are required (especially in portable applications), designers can make use of suspend mode, stop clock capability, and System Management Mode (SMM).

Other features include:

- PR-133 performance at 133 MHz
- 16-KByte Unified L1 Cache
- Integrated Floating Point Unit
- Enhanced System Management Mode (SMM)
- 64-bit FPM/EDO DRAM Controller

Major Functional Blocks

The MediaGX processor is made up of eight major functional blocks, as shown below:

- Execution Core
- Floating Point Unit
- L1 Cache
- Internal Bus Controller
- PCI Controller
- Graphics Pipeline
- Display Controller
- DRAM Controller

In general, data and code from DRAM or the PCI port travels over the X and C internal bus lines to the L1 cache where it is stored. Code instructions are fetched from the DRAM port or L1 cache by the execution core and floating point unit for processing.

Video data is processed by the graphics pipeline and video display controller. Output from the video display controller is sent to a CRT monitor (via a RAMDAC chip) or directly to a flat-panel monitor.

The PCI bus controller is used to control the PCI bus—there is no external CPU bus. The MediaGX Cx5510 performs functions such as interfacing to the IDE and I/O ports and the ISA bus.

Execution Core and Load/Store Unit

The Execution Core fetches, decodes and executes integer x86 code instructions. The decoupled Load/Store unit allows multiple memory accesses to be processed in a single clock cycle. Other features include single-cycle execution, single-cycle instruction decode, 16-KByte Write-Back cache, and clocks rates up to 133 MHz. This high performance is made possible by the use of advanced process technologies and execution core design that has many pipelined stages (superpipelining).

There are six pipeline stages:

- Instruction Fetch (IF)
- Instruction Decode
- Address Calculation 1 (AC1)
- Address Calculation 2 (AC2)
- Execute (EX)
- Write-Back (WB)

Write-Back allows data to be written to the cache and not immediately to main memory.

Branch Target Buffer

Often a software execution path loops through a set of instructions. The branch instruction at the bottom of the loop returns processing to the top of the loop except after the last loop iteration. The Branch Target Buffer (BTB) takes advantage of this phenomena and predicts correct branching more than 80% of the time.

Floating Point Unit

The Floating Point Unit (FPU) allows floating point instructions to execute in parallel with integer instructions and features a 64-bit data interface. The FPU incorporates a four-deep instruction queue and a four-deep store queue to facilitate parallel execution.

Unified Write-Back Cache

The 16-KByte Unified Write-Back cache is a data/instruction cache and is configured as four-way set associative. This L1 cache stores up to 16-KBytes of code and data in 1024 cache lines. The cache features a scratch-pad memory that allows selected cache lines to be used for the MediaGX VSA and graphics software. Scratch-pad memory lines, in some cases, greatly speed up multi-media instruction processing.

Internal Bus Controller

The Internal Bus Controller provides a bridge between the C bus and the X bus. The bus controller provides configuration control for as many as 20 different regions in system memory with separate controls for read access, write access, cacheability and PCI bus access.

PCI Controller

The PCI Controller is a full-function PCI interface module that supports cache line bursting, pacing of data during both read and write operations, permits up to three PCI masters and uses three types of arbitration.

Graphics Pipeline

The Graphics Pipeline is a full feature GUI accelerator that includes a complete bitBLT/rendering engine and support for all three-operand boolean raster operations. The graphics pipeline, controlled by a set of highly optimized Microsoft Windows 95 and NT drivers, provides outstanding GUI performance. The drivers and graphics pipeline are closely coupled in unique ways and have the capability to perform high-speed block transfers between virtual memory and the frame buffer.

Display Controller

The Display Controller interfaces the MediaGX processor to display devices. It provides direct interfaces to converts host data to TFT (Thin Film Transistor) flat panel displays and to RAMDAC (Random Access Memory Digital to Analog Converter) for driving CRTs.

The display controller retrieves image data from the frame buffer, inserts cursor and icon overlays into the pixel stream, generates display timing, and formats the pixel data for output to a variety of display devices.

Virtual System Architecture™ (VSA) Technology

A unique combination of hardware and software in the MediaGX provides compatibility with VGA and VESA graphic standards. The graphics pipeline and display controller are hardware assisted to support many VGA and VESA data operations, but all the of the VGA registers and controls are virtualized through Cyrix's Virtual System Architecture (VSA) software.

VSA technology allows hardware to be replaced by software without sacrificing compatibility. Hardware to be virtualized is replaced with simple memory and I/O trapping hardware. When an application or non-Windows operating system attempts to access a VGA register or memory range, the MediaGX processor detects the access attempt and internally takes a System Management Interrupt (SMI) and enters into a highly-optimized System Management Mode (SMM).

When the MediaGX goes into SMM, it saves the processor state and invokes a VSA handler that determines the cause of the SMI. The VSA handler then calls a VSA graphics driver to process the graphics access. The handler and VSA driver run in a special enhanced SMM mode making operations completely transparent to the application and operating system.

While VSA technology provides full compatibility for all VGA and VESA modes and registers, the VSA graphic drivers take full advantage of the graphics pipeline boosting VGA performance in the MediaGX.

The MediaGX also uses VSA software to provide compatibility with Sound Blaster audio standards.

MediaGX™ Cx5510 Feature Summary

♦ VSA Audio Controller

- Provides Sound Blaster® II, Pro and 16 Compatibility
- FM Synthesis
- MPU-401 MIDI Interface
- Audio Sampling with Data Formatting
- Upgradeable to Hardware Wave Table

♦ PCI to ISA Bridge

- Operates up to 40 MHz
- Supports PCI Initiator to ISA and ISA Master to PCI Cycle Translations
- Subtractive Agent for Unclaimed Transactions
- PCI INT[A:D] Support

♦ Additional Features

- 208-Metal Quad Flat-Pack (MQFP) Package
- 0.6 micron, CMOS Process
- Three-Layer Metal
- 3.3 Volt Core Operation
- 5.0 Volt ISA and IDE Interface Operation

♦ AT Compatibility

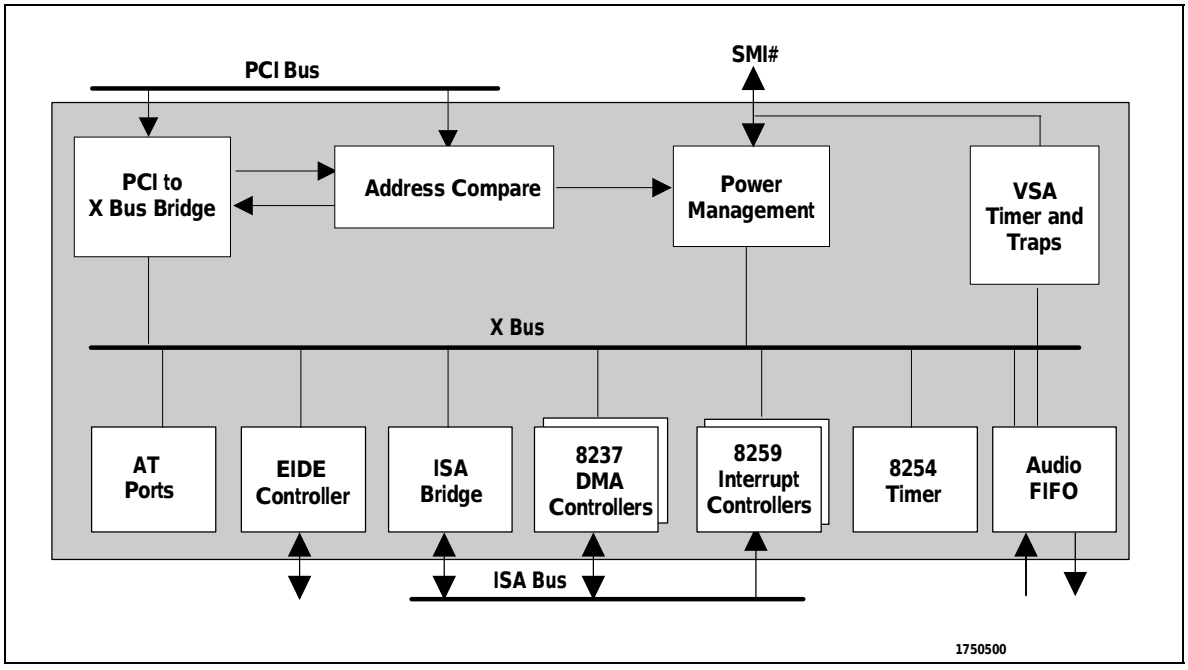
- 8259A Equivalent Interrupt Controllers
- 8254 Equivalent Timer
- 8237 Equivalent DMA Controllers
- Port A, Port B and NMI Logic
- Positive Decode for AT I/O Space
- Math Coprocessor Support
- Boot ROM and Keyboard Chip Select

♦ Power Management

- Automated CPU Suspend Modulation
- I/O Traps and Idle Timers for Peripheral Power Management
- Software SMI and Stop Clock for APM Support
- Up to Eight General Purpose I/Os for System Control
- Keyboard and Mouse Activity Detect
- Shadow Register Support for Zero-volt Suspend

♦ Bus Mastering IDE Controllers

- Two Controllers with Support for up to Four IDE Devices
- Independent Timing for Master and Slave Devices
- Four 32-Bit Prefetch Buffers and Write Buffers
- PCI Bus Master Burst Reads and Writes
- PIO Mode 4 Support
- Bus Mastering Supported for Non-DMA Drives



MediaGX™ Cx5510 Overview

The MediaGX Cx5510 represents a new generation of integrated, single-chip controllers for Cyrix's MediaGX line of x86-compatible 64-bit processors. The Cx5510 is a bridge to the ISA bus, performs traditional chip-set functions and supports a full-featured Sound Blaster®-compatible sound interface.

The Cx5510 provides a PCI version 2.1 compatible interface operating up to 40 MHz. The Cx5510 contains a PCI to ISA bridge.

For AT compatibility, the Cx5510 emulates two 8237 DMA controllers, an 8254 interval timer, and decode logic for AT register space. The Cx5510, in conjunction with the MediaGX processor and the VSA design, enables Sound Blaster® -compatible audio functions. The chip also provides a MIDI audio port and a two-channel (four-device) Bus Mastering IDE controller.

Full-function power management allows for notebook as well as desktop designs.

PCI Bus Interface

The Cx5510 provides a PCI Bus interface that acts as both a slave for PCI cycles initiated by the CPU or their PCI master devices, or as a master for DMA and ISA master transfer cycles. The Cx5510 generates address and data parity and performs parity checking It does not include the PCI bus arbiter. The arbiter is located in the MediaGX processor.

The Cx5510 contains configuration registers that are accessed through the PCI interface.

ISA Bus Interface

The Cx5510 provides an ISA bus interface for subtractive-decoded memory and I/O cycles on the PCI bus. The Cx5510 supports ISA Bus Masters through the DMA controller. The Cx5510 supports the standard ISA refresh function.

Power Management

The Cx5510 integrates advanced power management features including idle timers for common system peripherals, address trap registers for programmable address ranges (for I/O or memory accesses), three programmable general purpose external inputs, clock throttling with automatic speedup for the CPU clock, software CPU stop clock, zero-volt suspend/resume with peripheral shadow registers, and a dedicated series bus to and from the MediaGx microprocessor providing CPU power management status. The Cx5510 can virtually power the MediaGx processor off during a 3-volt suspend.

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